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Attorneys for Plaintiff
VERIGY US, INC.

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

VERIGY US, INC, a Delaware Corporation

Plaintiff,

vs.

ROMI OMAR MAYDER, an individual; WESLEY MAYDER, an individual; SILICON TEST SYSTEMS, INC., a California Corporation; and SILICON TEST SOLUTIONS, LLC, a California Limited Liability Corporation, inclusive,

Defendants.

Case No. C07-04330 RMW (HRL)

DECLARATION OF WEI WEI IN SUPPORT OF PLAINTIFF'S REPLY AND SUPPLEMENTAL BRIEF RE ORDER TO SHOW CAUSE RE PRELIMINARY INJUNCTION

Date: December 14, 2007
Time: 9:00 a.m.
Place: Courtroom 6
Judge: Hon. Ronald M. Whyte

Complaint Filed: August 22, 2007
Trial Date: None Set

HIGHLY CONFIDENTIAL – ATTORNEYS EYES ONLY

DOCUMENT SUBMITTED UNDER SEAL

I, Wei Wei, declare as follows:

1. I am a Managing Engineer for Exponent Failure Analysis Associates ("Exponent") and work in Exponent's Electrical and Semiconductors practice. I have been employed by Exponent since September 2004. I have been retained by Verigy Inc. ("Verigy") to provide technical opinions related to the development of Verigy's [redacted] Application Specific Integrated Circuit ("ASIC") chip and the development of the "Flash Enhancer" ASIC by its former employee, Romi Omar Mayder. It is my understanding that Mr. Mayder is currently the president and Chief Executive Officer ("CEO") of Silicon Test Systems, Inc. ("STS").

2. My analysis, reasoning and opinions are listed in the sections below. This report is based on information and materials made available to me. Should additional information or materials provide further insight, I reserve the right to amend my opinions.

EXECUTIVE SUMMARY

3. A summary of my conclusions is as follows:

[redacted]

4. My qualifications to testify on this matter are set forth in my curriculum vitae, a true and correct copy of which is attached as Exhibit A. In addition, my experiences that are specifically related to this matter are as follows. I have more than five years of experience related to integrated circuit design. I was a project leader for the research and development of programmable logic devices ("PLDs") using embedded NOR type flash memory array at Atmel Corporation. My responsibilities included chip architecture design, floor planning, memory read and program circuit design, I/O circuit design, and layout. I was also the technical lead for a Multiple Chip Module ("MCM") that included a CMOS ASIC chip. This MCM was designed as a configuration memory for Field Programmable Gate Array ("FPGA") devices. My responsibilities included creating ASIC chip design specifications, performing design implementation and verification of the ASIC chip using Hardware Description Languages ("HDLs") such as Verilog, performing logic synthesis using a standard cell library, and designing and implementing FPGA emulation chips to verify and test the functionality of the ASIC design.

5. During my role as a project leader for the embedded NOR flash PLD designs, I worked closely with product and test engineers to resolve technical issues during wafer sort, final test, and in the field. I have operated manual wafer probe stations to test and debug silicon wafers, and I have operated Automatic Test Equipment ("ATE") for both wafer and package tests. I was also involved in the modification of test programs for these products during the engineering debug

phase. During my role as the technical lead for the configuration memory ASIC development, I worked closely with marketing personnel in the product definition phase and also worked closely with test engineers to define testable features in the MCM. During these design projects, I also worked closely with packaging engineers to select package types, specify the die size, bond pad size and bond pad arrangement, and finalize package drawings for the IC chips that I developed. I have also worked on several projects related to embedded NOR Integrated Circuit (IC) chips and NAND flash memory technology since I joined Exponent.

TECHNICAL BACKGROUND

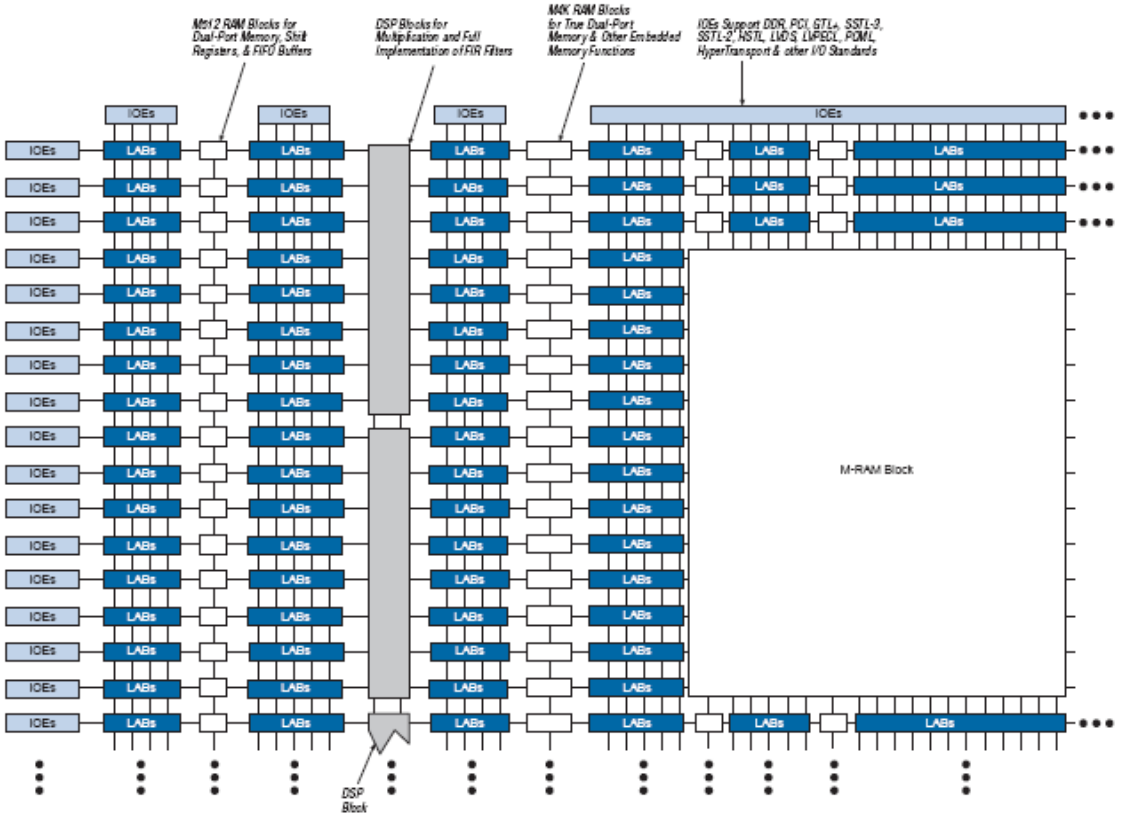
6. **ASIC** An Application Specific Integrated Circuit ("ASIC") is a chip customized for a special purpose. It is designed to solve a specific problem or for a special application that cannot be as efficiently addressed by publicly available standard off-the-shelf chips. For example, a video decoder may be made of a combination of discrete logic components such as logic gates, flip-flops, multipliers, multiplexers, and to realize a special compression/decompression scheme. Because a decoder made of these discrete components cannot meet the specific requirements for the application, for instance, speed performance is too slow, power dissipation is too high, or the total circuit might be too big to fit in the TV box, an ASIC chip is developed to meet these specifications. Each of the functional blocks in this ASIC have may have a functionally equivalent off-the-shelf standard component. However, the combination, and the process of combining these well-known functionalities and realizing them on a single chip, provides a unique solution that solves a specific problem. To maintain a competitive advantage, the design specifications for developing an ASIC are typically kept as confidential information.

7. Typically, a system integrator such as Verigy would have an idea for an ASIC design at the high level, formulate high level engineering specifications, and contract a semiconductor design house that offers ASIC design services to further develop and produce this chip. Companies such as Atmel and LSI Logic provide such services.

8. **ASIC vs. FPGA** A type of modern day standard off-the-shelf logic chip is called a Field Programmable Gate Array ("FPGA"). It competes directly with logic ASICs in many applications. The market leaders of FPGAs are Xilinx and Altera. FPGAs from both companies

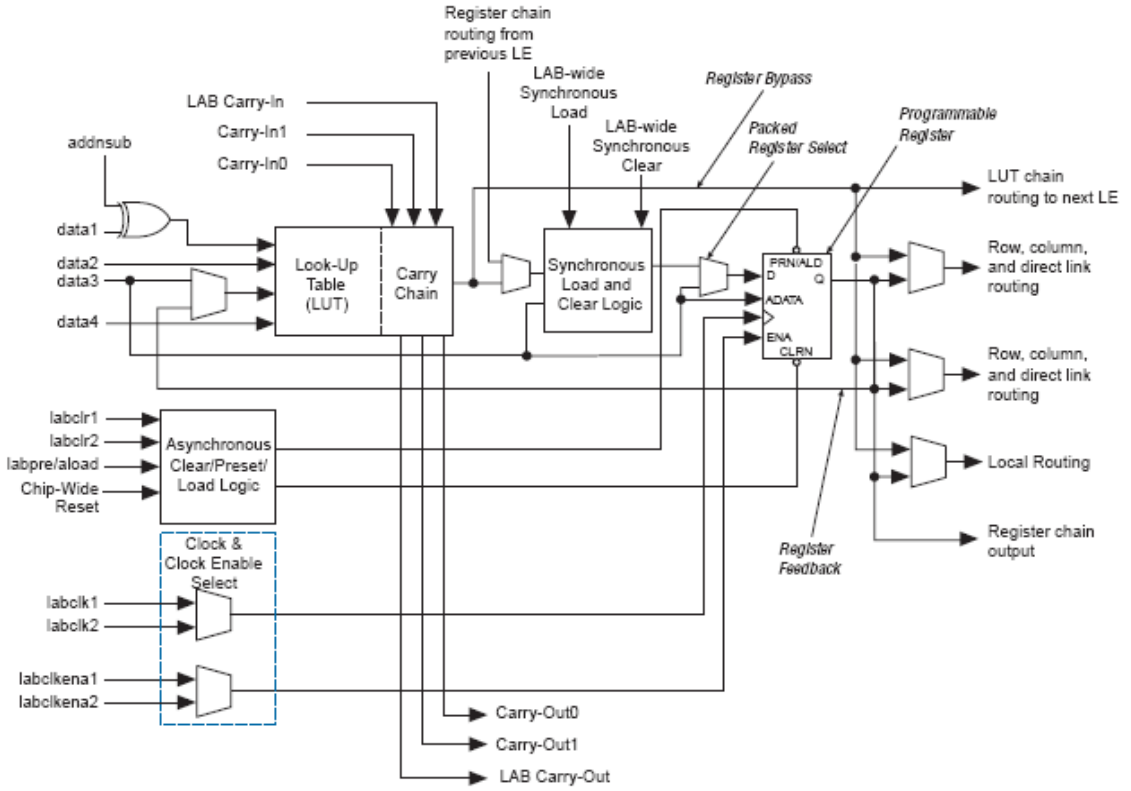
are fabricated on standard low voltage CMOS processes. Leading edge FPGAs operates at supply voltages in the 1.1 V to 1.8 V range while some legacy products may offer support for higher voltages up to 5V. A block diagram of an Altera Stratix FPGA is shown below.

Figure 2–1. Stratix Block Diagram



9. A description of the Stratix FPGA from its datasheet is quoted here: "Stratix devices contain a two-dimensional row- and column-based architecture to implement custom logic. A series of column and row interconnects of varying length and speed provide signal interconnects between logic array blocks ("LABs"), memory block structures, and Digital Signal Processing ("DSP") blocks. The logic array consists of LABs, with 10 logic elements ("Les") in each LAB. An LE is a small unit of logic providing efficient implementation of user logic functions. LABs are grouped into rows and columns across the device." The block diagram of one LE is shown below.

Figure 2–5. Stratix LE



10. In a FPGA, The LE, the interconnections that connects the LEs, the I/O structures are all programmable and can be re-configured. The configurations of the programmable LE, interconnect, and I/Os are stored in latches or Static Random Access Memories (SRAMs) that can be reprogrammed even after the device is installed in a system. *The FPGA configuration files, which determine the final functionality of the device, are considered intellectual property that the users created for their designs. They are highly guarded secrets.* FPGA manufacturers offer encryption and other means to protect the content of the configuration from being misappropriated by adversaries.

11. The density of the FPGAs can be very high. For instance, the EP1S80 device has 79,040 LEs, 7 Mb Random Access Memory ("RAM"), 22 DSP blocks, 176 embedded multipliers, and 1,238 I/Os. The device is not designed for manual configuration. Sophisticated design software is provided for the FPGA users to implement their design. For example, Quartus II is software offered by Altera to develop products based on their FPGAs. These FPGAs, along with the software design support, offer great flexibility in circuit design and provide a significant

amount of ready to use resources, and can be re-configured much quicker than going through a lengthy silicon process such as the ASIC design. Many times, FPGA becomes the prototype tool for advanced logic ASIC design because of its versatility and programmability and some time even become direct implementation choices if the cost/performance is justified. However, the decision of whether to use an ASIC or FPGA is multi-faceted – and the decision typically boils down to:

- *Can FPGA implement this solution?* FPGA focuses on standard low voltage logic applications such as decoders, signal processing and controllers. It does not focus on analog components or special purpose performance blocks, such as high voltage applications.

- *Can FPGA implementation meet the performance requirements?* Speed and power constraints are all part of the evaluation. Even though the FPGA offers a lot of flexibility, it is still a fixed structure and has its limitations. Also, because of its diversity, it may not be optimized for certain specific constraints and is difficult to use in those applications. In these cases, the ASIC design is still the ultimate choice.

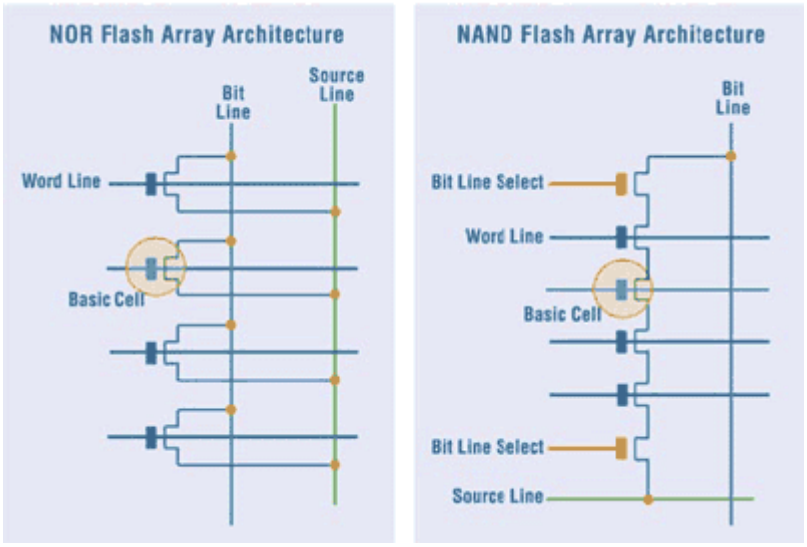
- *Can the cost of the ASIC/FPGA be justified?* Forecasted volume, manufacture cost, and NRE cost are all factored in to make that decision. A FPGA, because of its versatility, some times contains too much redundancy resources than a straightforward ASIC design and ends up costing more.

12. **Flash Memory** Flash memories are Non-Volatile Memories ("NVM") that can be electrically programmed and erased. In a NVM, once the information is stored in the memory cell, the memory cell retains the information it stores without electrical power supply. On the contrary, volatile memories such as Static Random Access Memory ("SRAM") and Dynamic Random Access Memory ("DRAM") lose the information stored in the memory when the power supply to the memory is removed. Flash memories find their applications in cell phones, computers, digital cameras and many other consumer appliances and have a large worldwide market.

13. The information is stored in the flash memory cell by a "PROGRAM" operation or an opposite "ERASE" operation. The "PROGRAM" operation is also referred as "WRITE". The information stored in the flash memory cell is retrieved by a "READ" operation. *Compared to the "READ" operation, the "PROGRAM" and "ERASE" operations are orders of magnitude slower and require higher electrical voltages applied to the cell structure* so the electric charges can be

transferred to the floating gate storage structure in the cell. In modern flash memory devices, the high voltage (typically 10 V and above) is generated inside the device and converted from the low voltage power supply of the chip (typically 5 V and below).

14. There are two main types of flash memory architecture to group the flash memory cells together: NOR and NAND. Both NOR and NAND flash memory use the floating gate structure and require high voltage during the "PROGRAM" and "ERASE" operations. Conceptual schematics of the NAND and NOR structures are shown below. This diagram is reproduced from an April/May 2006 issue of Chip Design Magazine article, entitled "Flash Memory Moves from Niche to Mainstream," authored by Francois Kaplan, a true and correct copy of which is attached as Exhibit K:



15. Because of differences in cell organization between the NAND and NOR arrays, NAND memory can achieve a higher density than NOR memory, but sacrifices the random access read operation speed. NAND memory is typically accessed in burst or page read mode to overcome this deficiency. In page mode, the data stored in an adjacent address is automatically read out in sequence. The penalty of slow random access read time occurs only at the first byte and the subsequent read access speed for NAND memory is on the order of 20 ns, very close to the NOR memory access speed. Therefore, if large data are stored in adjacent addresses in a NAND flash memory, the overall access time in page mode is comparable to that of a NOR flash memory.

16. There are some differences between the NOR and NAND flash memories from a user point of view. They are listed in table 1 on page 8 of Dr. Richard Blanchard's declaration. However, the differences between NAND and NOR flash memory are also device and manufacture specific. For example, there is a type of *Low Pin Count ("LPC") NOR flash memory* that has a serial interface with pin counts similar to that of a NAND flash memory. A true and correct copy of the SST49LF016C LPC NOR type serial flash memory datasheet is shown in Exhibit B. Also, there is another type of *serial interface NOR flash memory* that has even lower pin counts than NAND memory. A true and correct copy of an Intel serial flash memory datasheet detailing such a device is shown in Exhibit C.

17. **Flash Memory Testing.** Flash memories, like many other semiconductor devices, are fabricated through many steps. Major milestones during the production process include: wafer processing, wafer sort test, packaging, and package level test. The wafer processing is a multiple step process to form flash memory cells, other peripheral transistors, and interconnection of these devices together to perform the intended function on a silicon substrate. Generally, these silicon wafers contain hundreds of identical flash memory chips (or dice) and each chip (or die) consists of millions or billions of memory cells. All chips are tested at the wafer level to sort out GOOD and NO-GOOD dice, hence the name wafer sort ("WS"). The NO-GOOD dice are rejected and marked on the wafer. The tested wafers are subsequently shipped to the assembly houses where the wafer is broken into individual dice through a process called die singulation using a diamond saw, and is ready for packaging. Only un-marked, GOOD dice are packaged. The packaging process involves encapsulating the dice in plastic or ceramic material to protect the silicon and form interconnections between the silicon die and the pins on the package so the device can be electrically accessed through these pins from outside the package. After the packaging process, the devices are tested again to sort out their different performance ratings, reject any defective dice introduced during assembly, shipping and handling, or missed during wafer sort. This process is typically referred to as final test ("FT"). The devices are subsequently marked with appropriate identification markings and are ready to be shipped to customers and be used in electronic applications such as a cell phone.

18. Automatic Test Equipment ("ATEs"), such as Verigy's V5400 and V5500, are used in wafer sort and final test. An ATE typically consists of tester control units, Algorithmic Pattern Generators ("APG"), Device Power Supplies ("DPS"), Source Measurement Units ("SMU"), memory, and Pin Electronics ("PE"). PE is sometimes referred as the test channel. The heart of the ATE testing is the test program software. The test program software consists of specially designed patterns and algorithms to evaluate the DUTs in a cost efficient manner. The ATE (or tester system) is a hardware that executes the test program software to evaluate the devices and relies on the software to make a decision based on the response from the DUT.

19. For wafer sort, a probe card is used to connect test channels and power supplies to the corresponding pads on DUTs ("Device Under Test") on the wafer. This is done through traces on the probe card circuit board and a customized array of miniature probe tips that make contact with the pads. The final test uses handlers that consist of many sockets. These sockets adapt to appropriate package types and form connections between DUT pins and tester resources.

20. Selecting tester resources and assigning them to different pads or pins on the DUT are integral parts of the test program design. They are device, tester and manufacturer specific. The tester channel assignments and device test programs are confidential information of the memory vendors. There are manufacturer-only test modes that operate the flash memories in ways that are not made public. They are used specifically to accommodate special testing purposes only. Entering these manufacturing test modes requires using certain pins in a non-conventional way that is not specified in product datasheets or made available to the general public – for example, applying high voltages on pins that are specified as low voltage pins in the public product datasheet. These manufacturer test modes are highly guarded trade secrets. For instance, there may be test modes that allow the manufacturer to change a certain configuration or device manufacture ID of the flash memory. *Because a test channel assignment may reveal how and which pins are used for these classified manufacture test modes, tester channel assignments are also highly guarded secrets.*

21. By testing multiple DUTs in parallel, a higher throughput can be achieved, thus reducing the overall COT ("Cost of Test"). Increasing throughput or parallelism can be achieved

both on the test equipment side and on the probe card or handler side. Various tester resource-sharing schemes are used, including multiplexers and or simply fan outs, many of which are discussed in page 11 to page 18 of Dr. Blanchard's declaration.

22. Both the NAND and NOR flash memory test programs typically consist of the following:

- DC (Direct Current) testing and parametric testing to screen out gross failures
- AC (Alternating current) Read/Command Interface test
- Algorithmic state machine test (logic test)
- ERASE operation performance test
- PROGRAM operation performance test
- ERASE/PROGRAM operation disturb test
- Redundancy test: diagnosis and repair

23. While there are differences between NAND and NOR flash memories, the differences generally affect the final user application. During manufacturer testing, this difference is reflected and addressed in test program software. As described in previous sections, the test program software is at the heart of the automatic testing. It consists of specially designed patterns and algorithms to evaluate the DUTs in a cost effective manner. Special test modes are sometimes build in the flash memory chip itself to improve test efficiency. These test modes are referred to as Design for Test ("DFT") features. Because of the leverage of special test modes and carefully designed test program software, the COT per chip of NAND and NOR can be very comparable.

24. The "random access read speed" and the "pin density" difference between NAND and NOR are of dubious importance in testing of NAND and NOR flash memories. First, the random access read speed difference is not a critical factor during wafer sort, as device read speed is not characterized during wafer sort and random access is not a must-have test feature in the test program. Also, as Dr. Blanchard stated in his deposition, line 3 to12, page 183, the PROGRAM (or WRITE) operation is 3 or 4 orders of magnitude slower than that of READ. The PROGRAM operation is the most time-consuming part of the test and the main contributor to COT, which is true for **both** NAND and NOR flash memory. Second, the number of pins on a NOR flash memory may not always be higher than that of a NAND flash memory. As mentioned earlier, A LPC NOR flash memory has a serial interface comparable to that of a standard NAND memory.

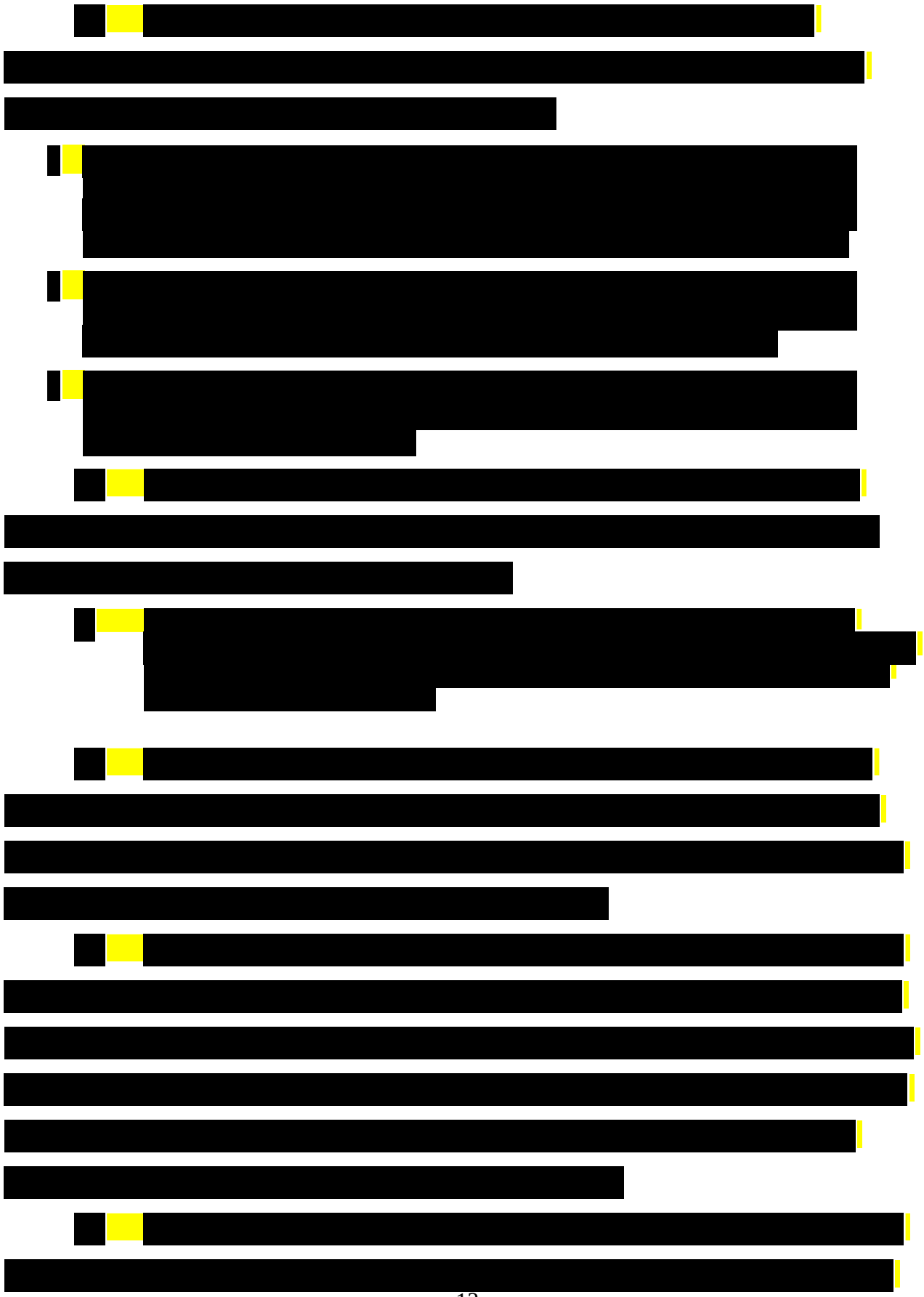
There is also a serial NOR flash memory that has only eight pins total, even less than that of a standard NAND flash memory.

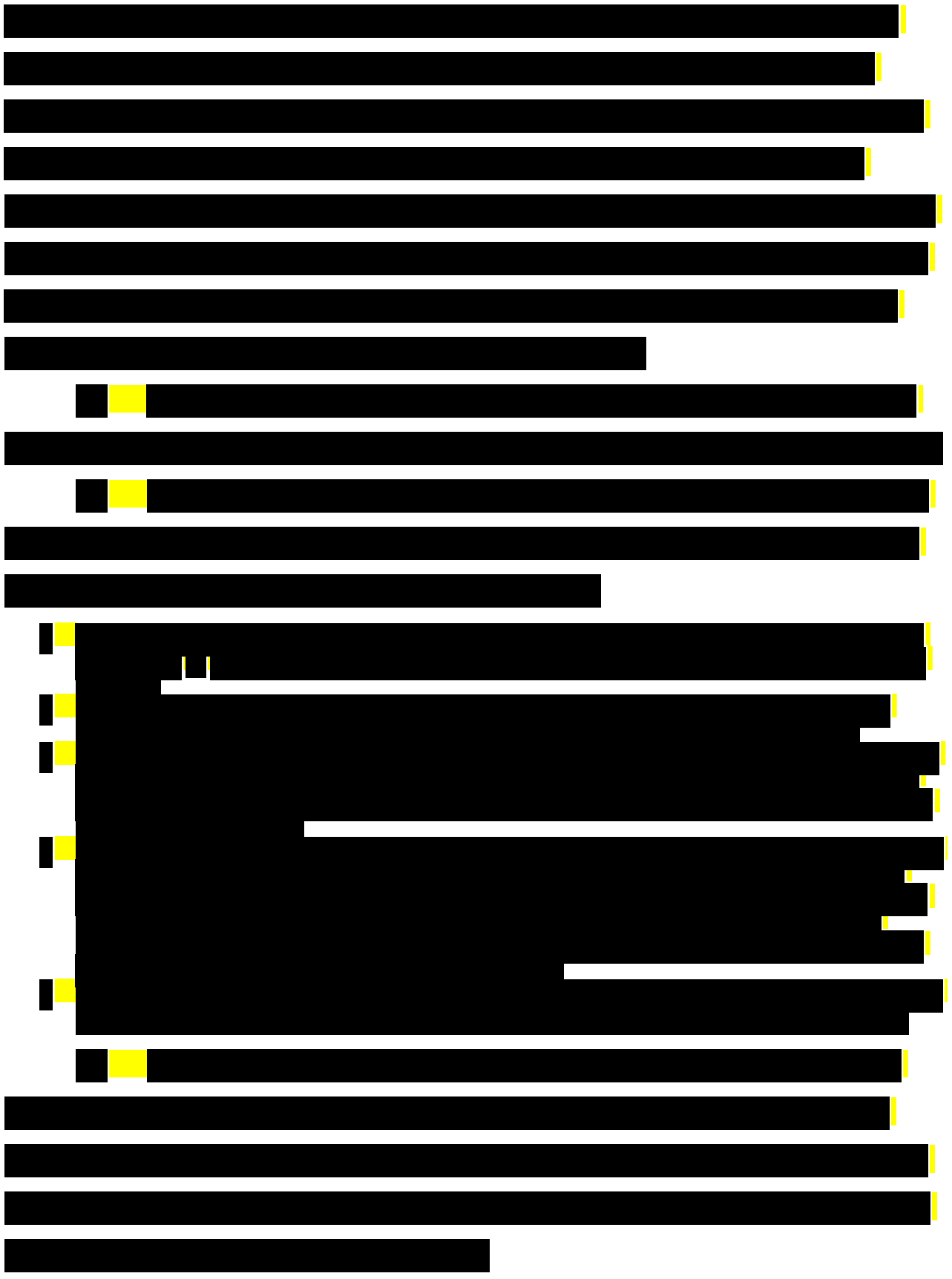
25. During a parallel testing configuration, the "resource sharing" hardware multiplexes or fans out the tester resources to multiple DUTs so they can be tested at once. The objective of this "resource sharing" hardware is to connect the tester resources to the DUT pins/pads in an effective manner with minimal degradation of the tester performance. The differences between NAND and NOR memories *are specific to the DUTs and test software programs only*. The "resource sharing" hardware provides connection and re-routing capabilities to support the execution of the test program software, regardless of whether the test program is for NAND or NOR flash memory. For instance, during Dr. Blanchard's deposition when he addresses "bit flipping" testing during wafer sort (line 15, page 183 to line 2, page 186), he stated that a "resource sharing" ASIC provides access to the chip. It doesn't make a judgment about the quality of the data read from the chip" (line 25, page 185 – line 2, page 186).

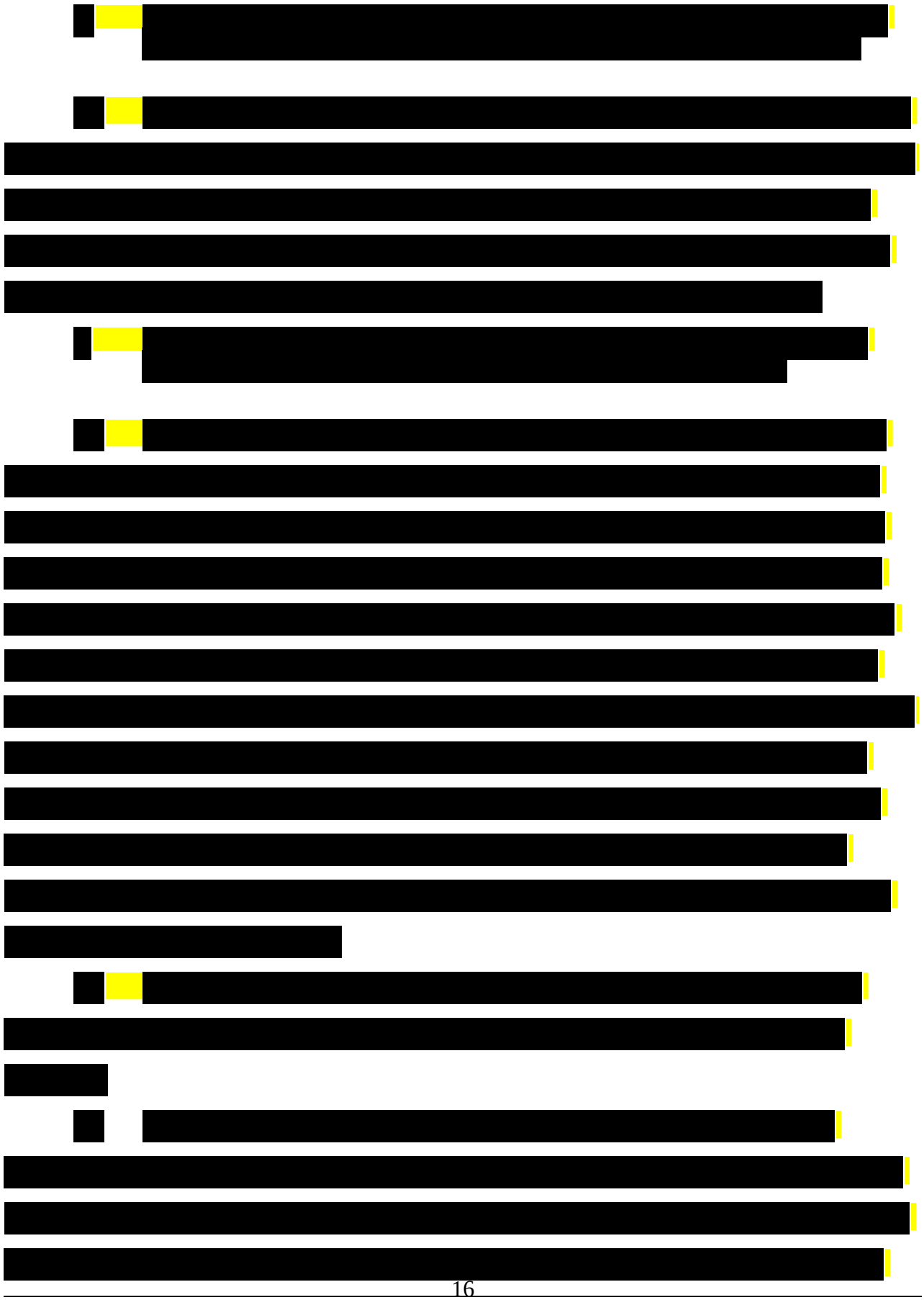
[redacted]

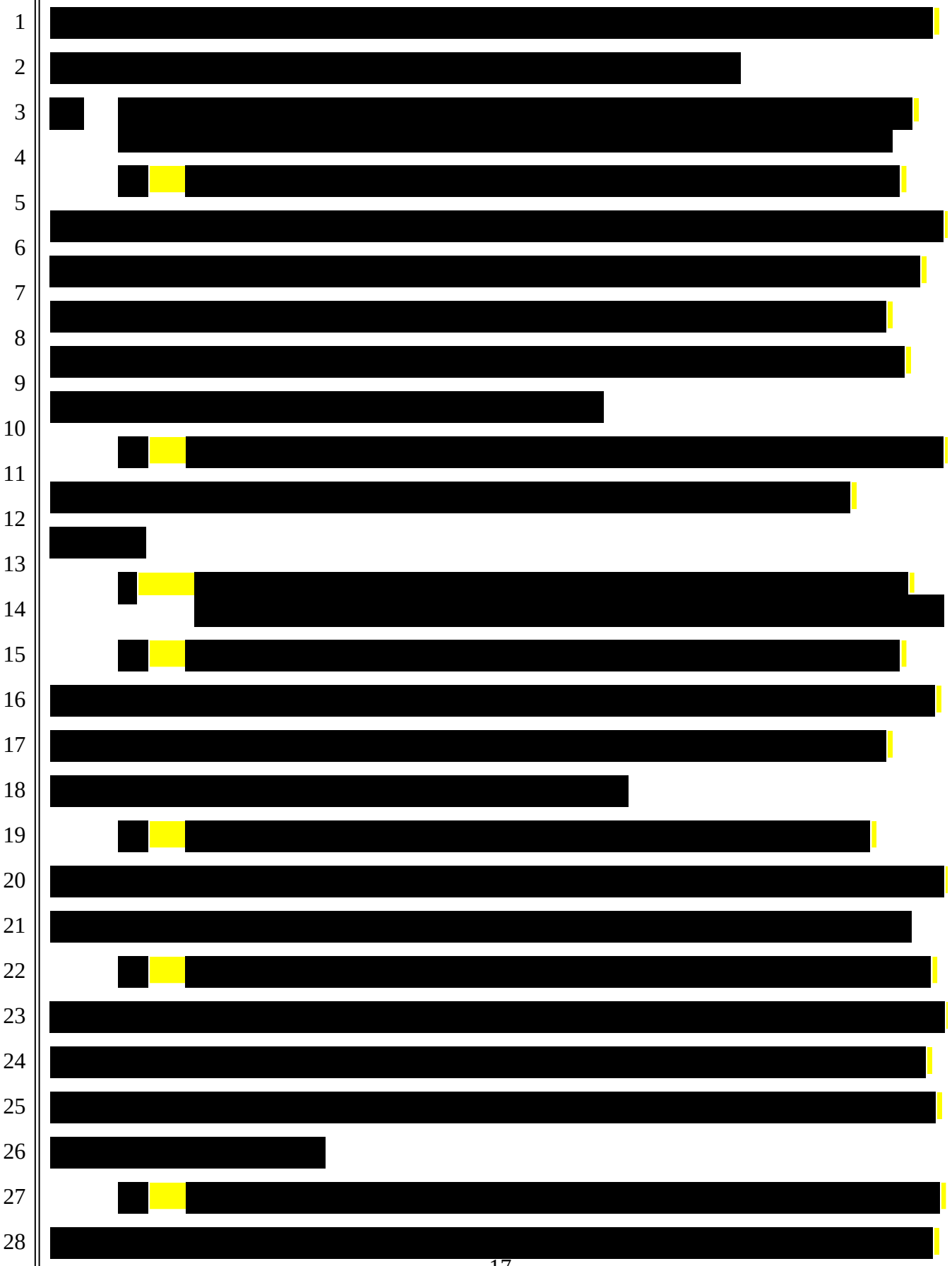
/ / /

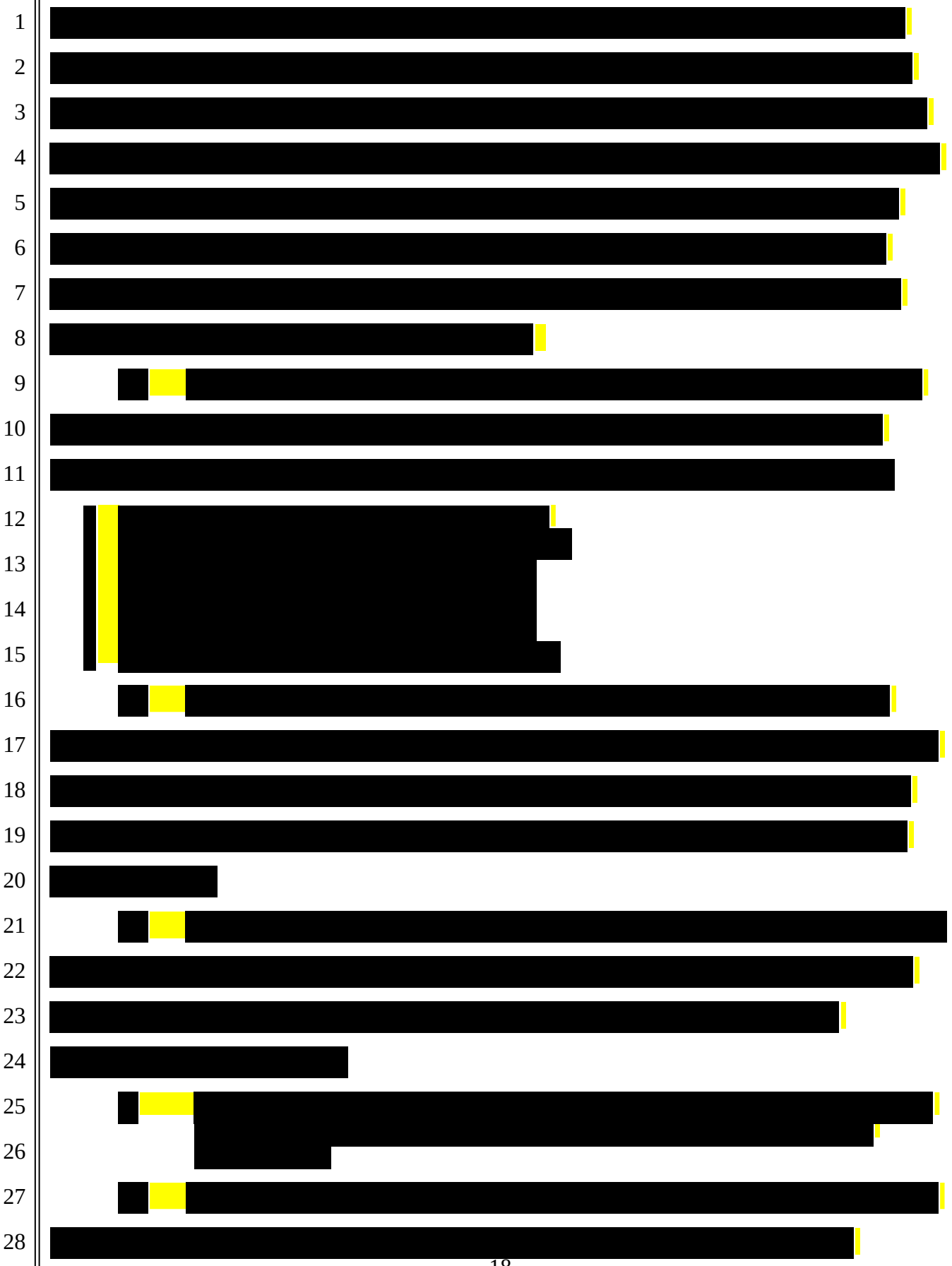
I. [redacted]

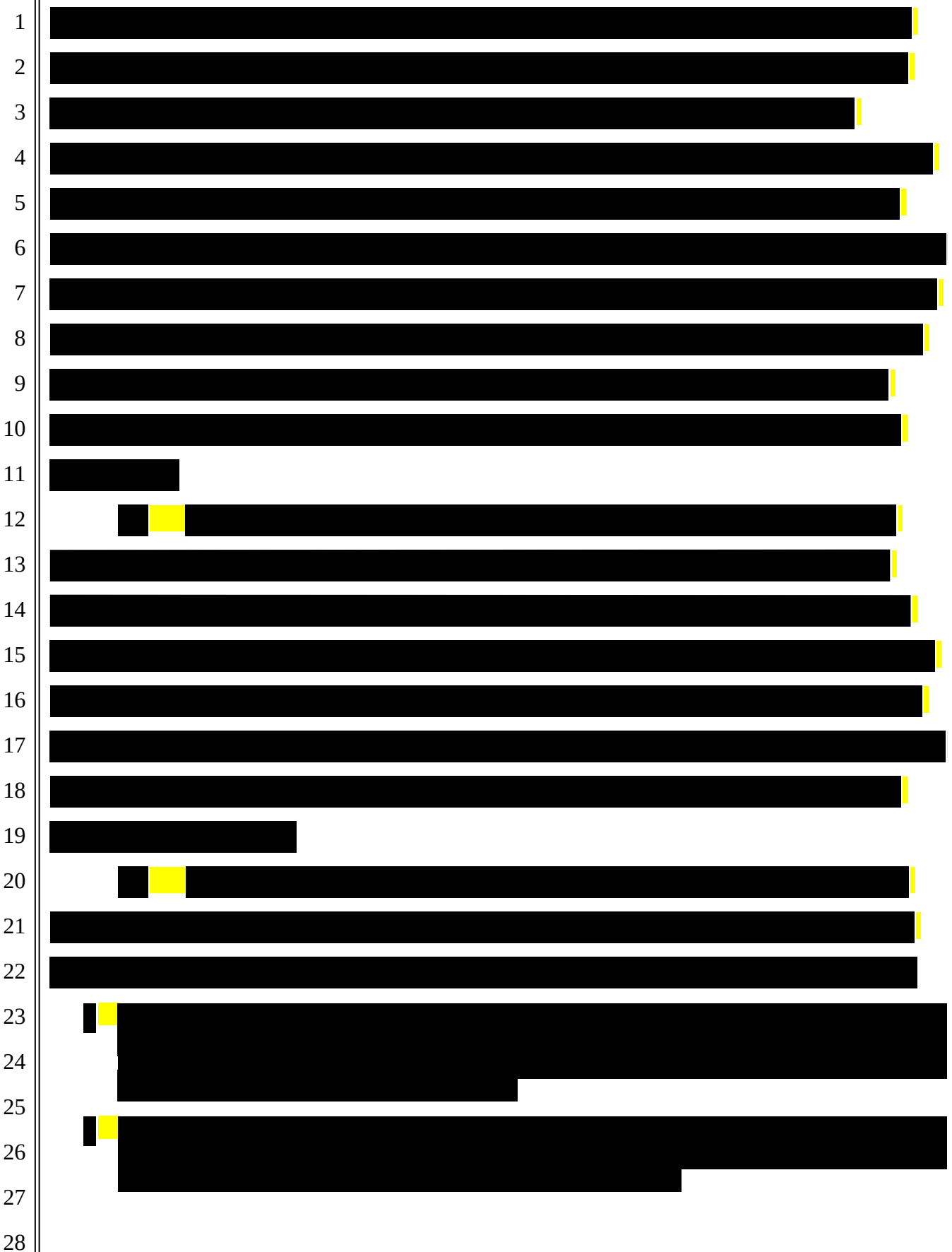


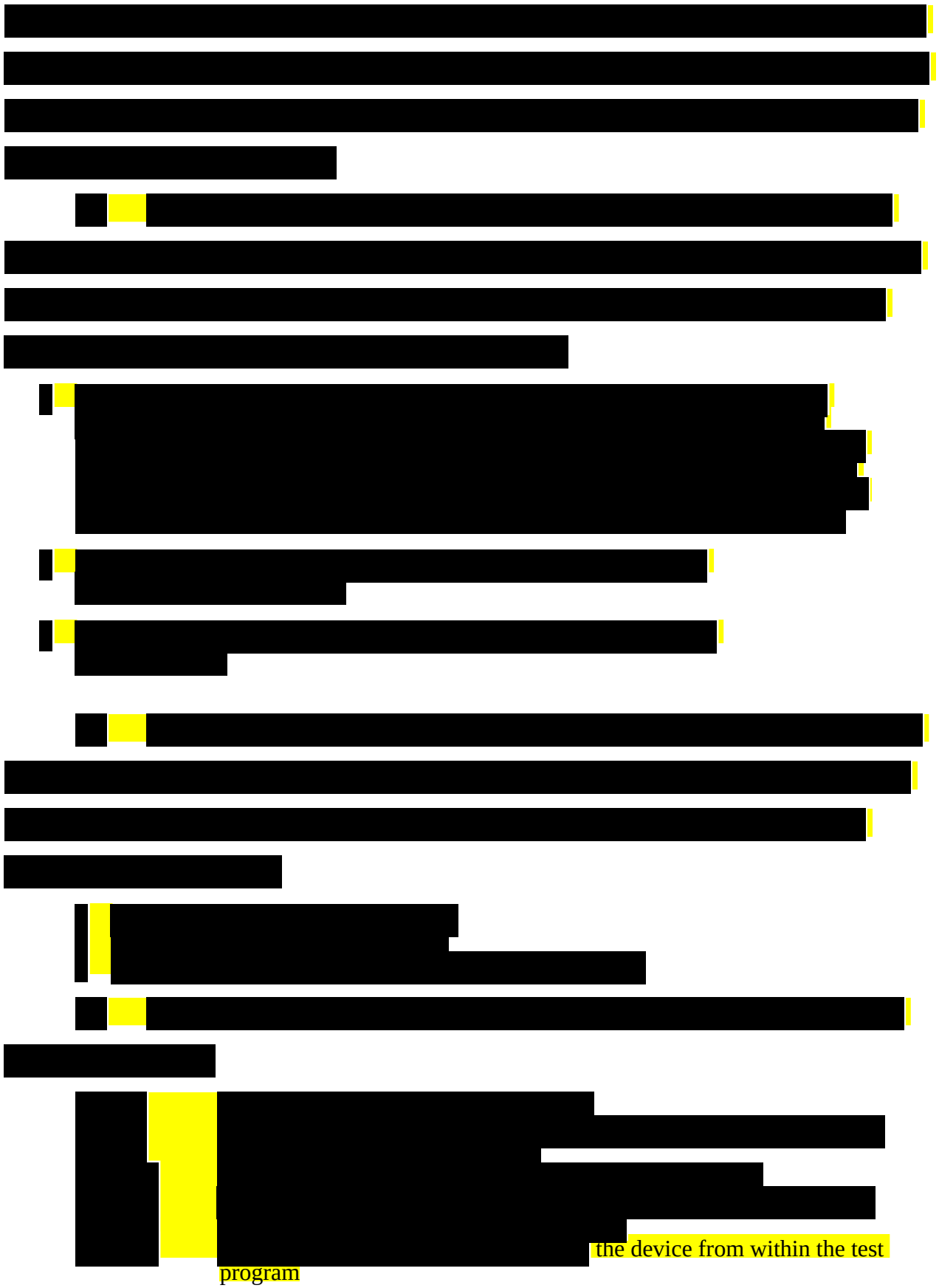




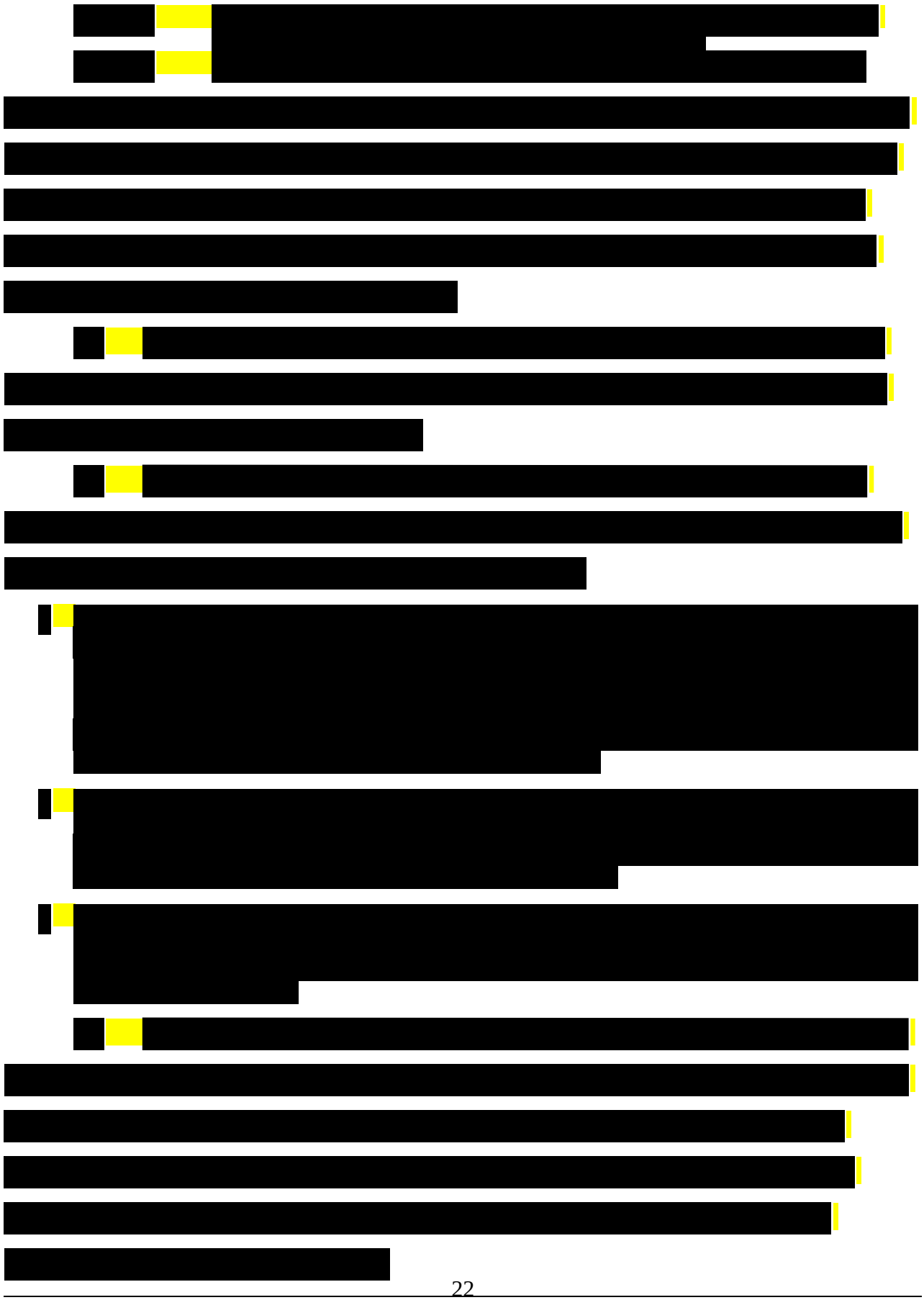


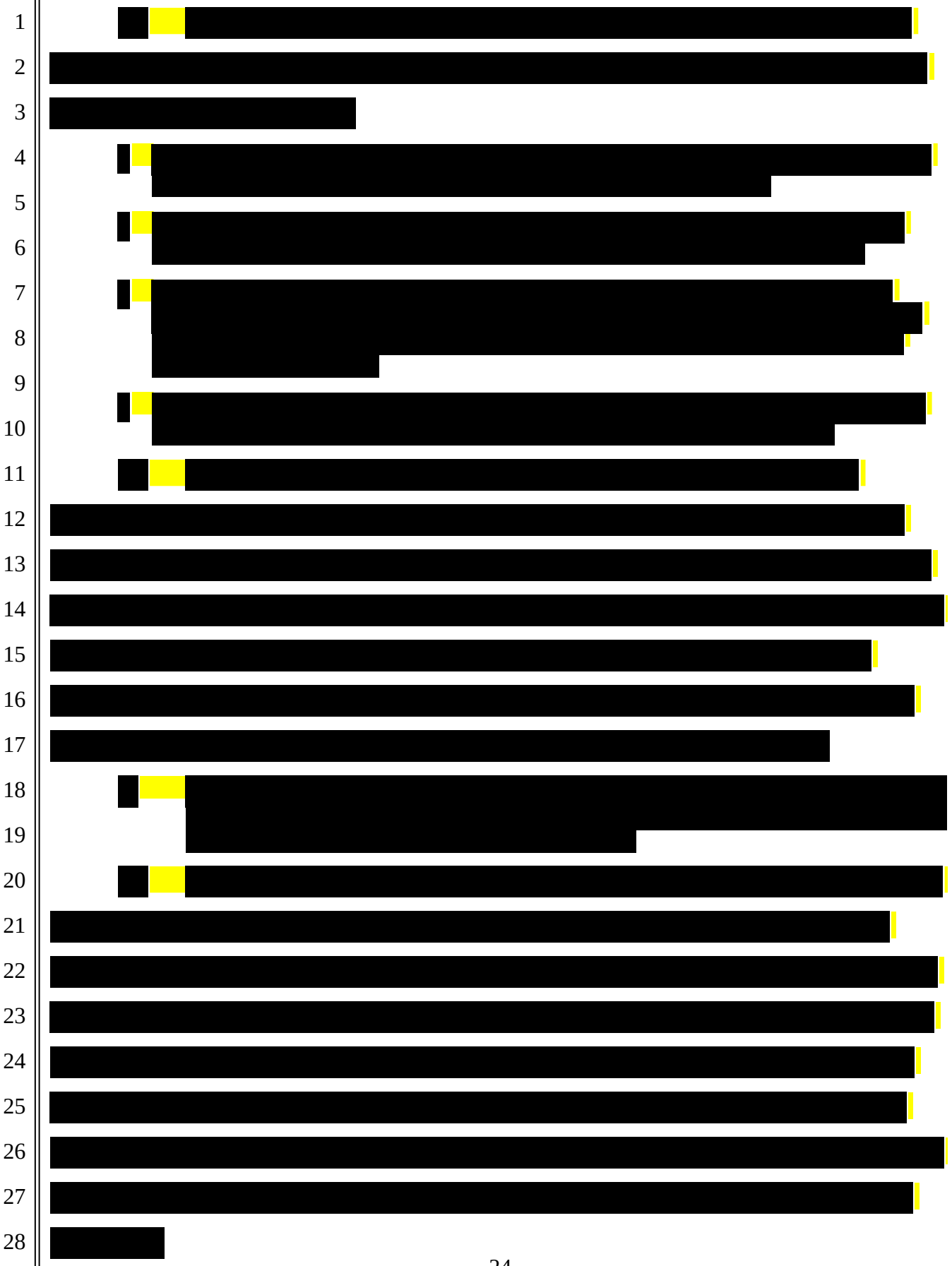


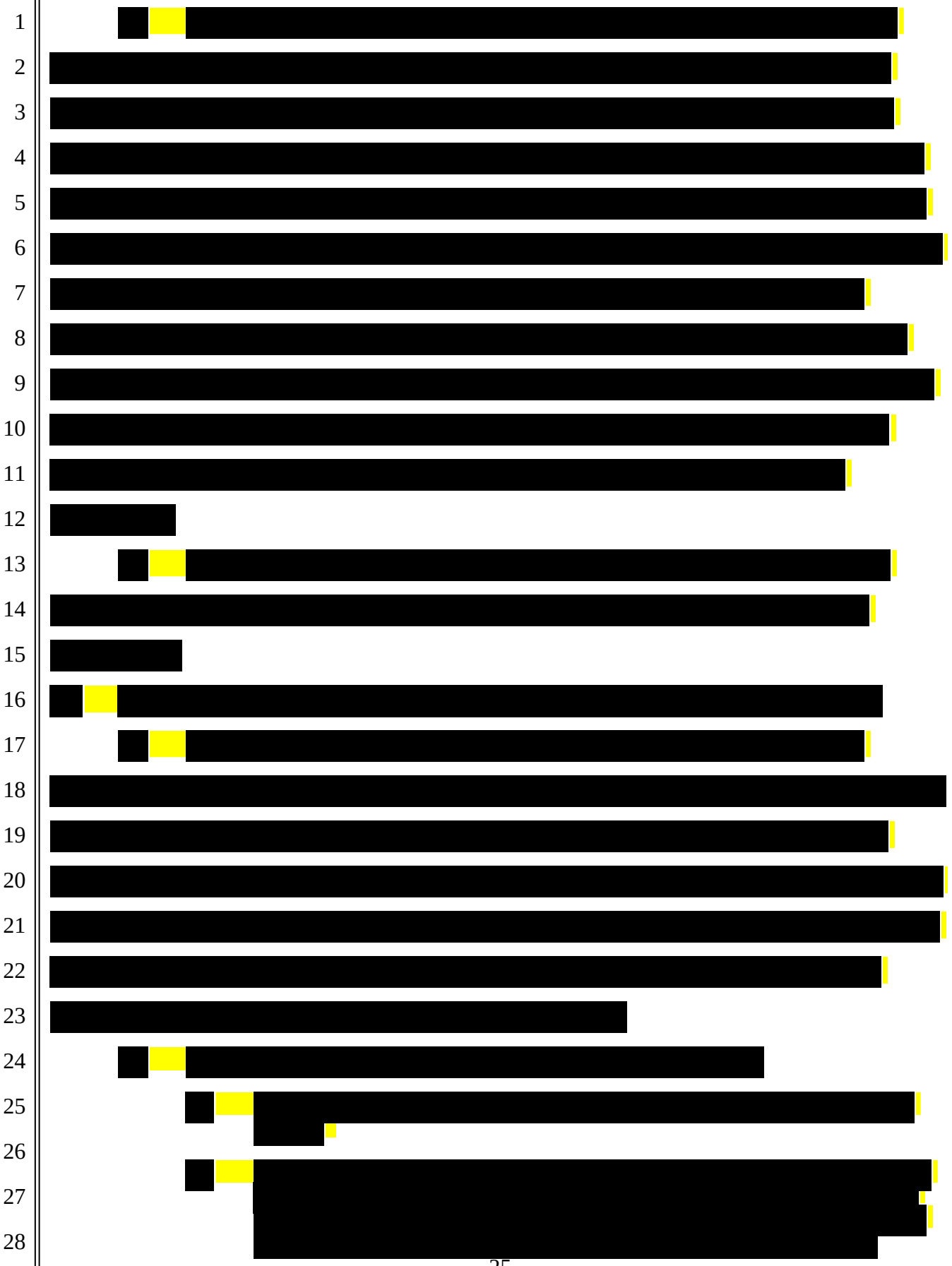




the device from within the test program







87. I have reviewed the public disclosure information provided in the Blanchard Declaration and the Declaration of Thomas Schneck. True and correct copies of the relevant exhibits from the Blanchard declarations are attached hereto as Exhibit I. True and correct copies of the Schneck Declaration plus relevant exhibits are attached hereto in Exhibit J. Based on these documents, which disclose certain references which are addressed below, I did not find a publicly disclosed solution that is the same as

88. ***US patent application 2006/0170435***. This patent application, titled "Programmable Devices to Route Signals on Probe Cards", was filed by Form Factor on January 31, 2005 and was published on August 3, 2006, several months after the RFQ of the Chameleon ASIC was formed. This application issued on July 17, 2007 as US Patent No. 7,245,134. In this patent, a FPGA chip was disclosed to act as a programmable switch matrix to re-route test channels to DUT pins on a probe card. A copy of the schematic diagram of the solution disclosed in this patent application is shown below:

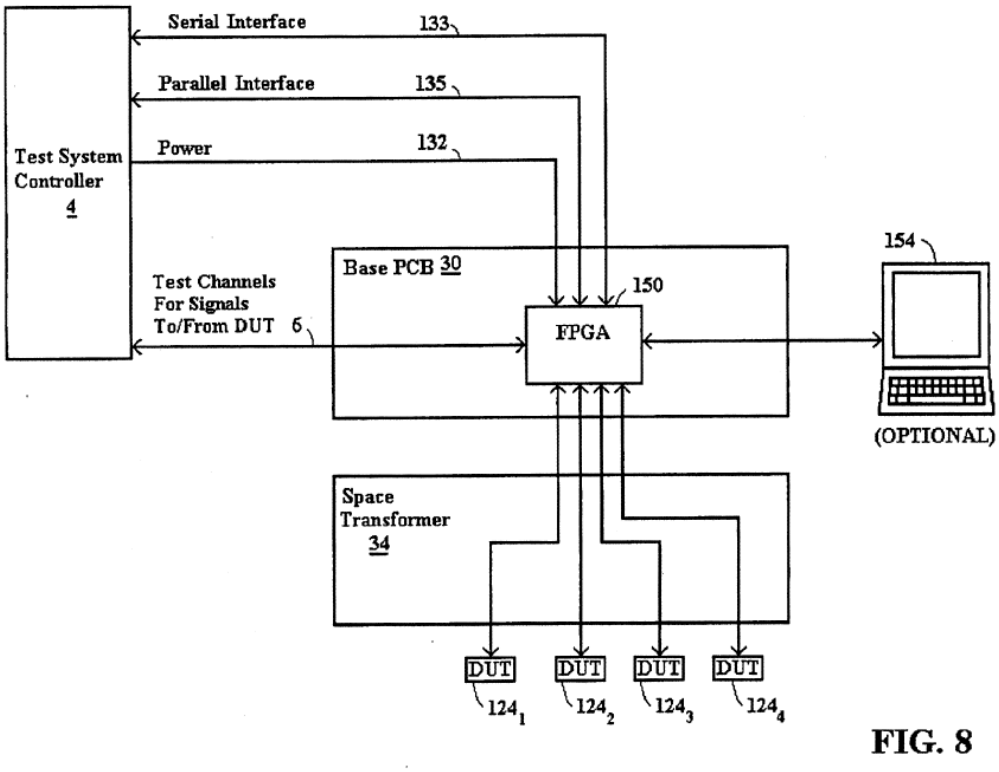
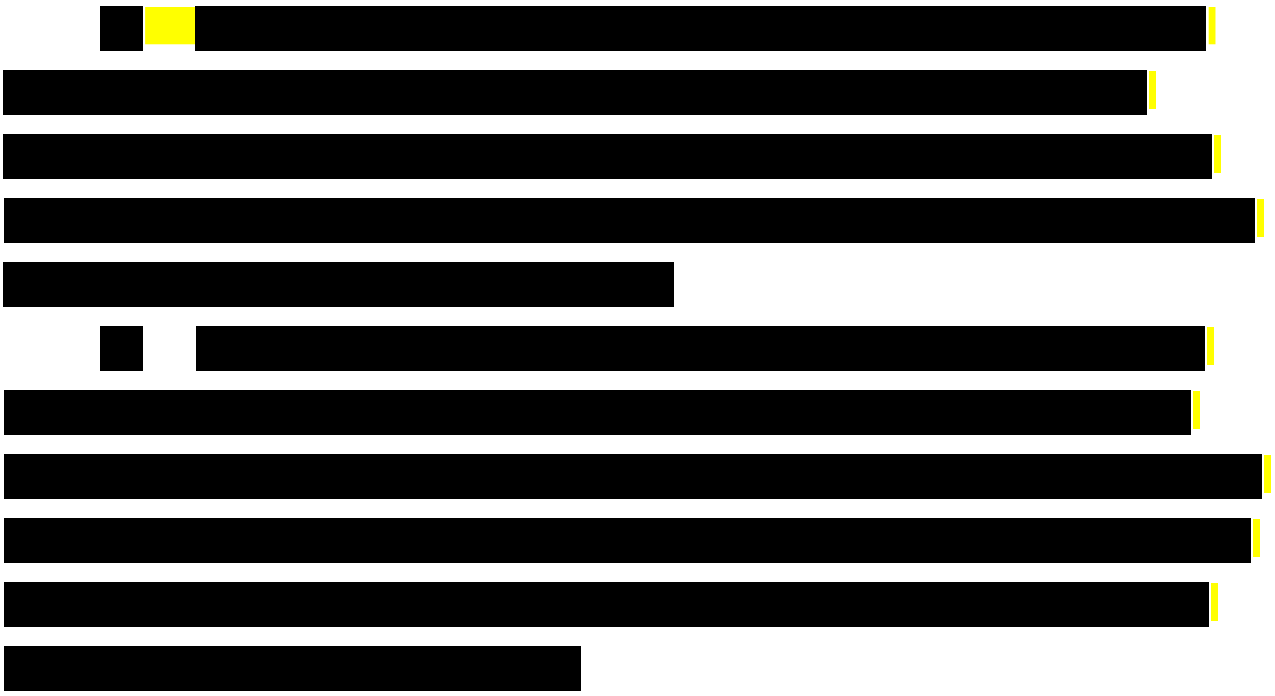


FIG. 8

Patent Application Publication Aug. 3, 2006 Sheet 5 of 6 US 2006/0170435 A1

Figure 8 of the 2006/0170435 patent application

[redacted]



93. ***US patent application 2005/0237073***. This patent application, titled "Intelligent Probe Card Architecture", was filed by FormFactor on April 21, 2004 and published on October 27, 2005. In one embodiment of the invention disclosed in this application, it described a probe card system with a probe card daughter board (item 100 on Fig. 7) that contains the fan out of the power signals using discrete DC/DC converters and voltage regulator, a FPGA or other programmable logic device to re-rout the fanned out power and other scan chain test signals, and additional discrete multiplexes to read the output of the DUTs and space transformer to fan out the input signals of the DUTs. An illustration of the solution disclosed in this patent is shown below.

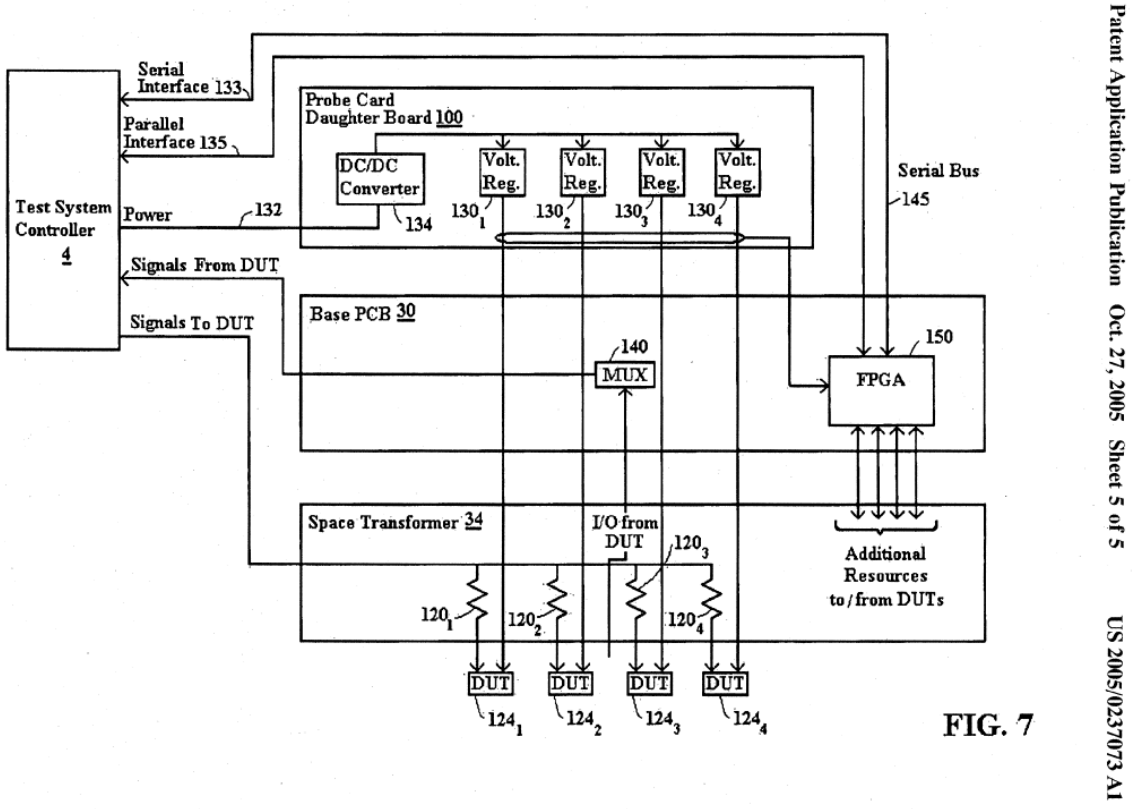


FIG. 7

Figure 7 of the 2005/0237073 patent application.

94. The solution disclosed in this patent is not the same as the Chameleon ASIC. It does provide a solution where the programmable switch matrix and the programming interface are in the same chip, such as the Chameleon ASIC has. But the FPGA is used in combination with the multiplex and fan out max. It does not contain a solution made of a combination of SPST switches arranged in the same topology specified in the Chameleon ASIC. Therefore, it is a different solution than the Chameleon ASIC.

95. ***US Patent No. 6,366,112 B1.*** This patent, titled "Probe Card having on-board multiplex circuitry for expanding tester resources", was filed by Micron on October 9, 2001 and issued on April 2, 2003. It described a probe card contact interface made of silicon to form the probe card – a DUT contact and a multiplex circuit that can be either fabricated on the same substrate or on a different substrate, but be solder bumped onto the probe card contact interface silicon. Key features of this patent are shown below.

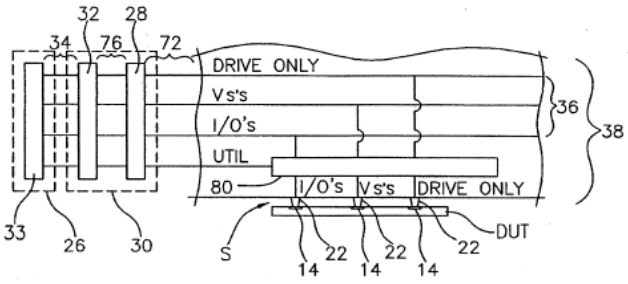


FIGURE 8A

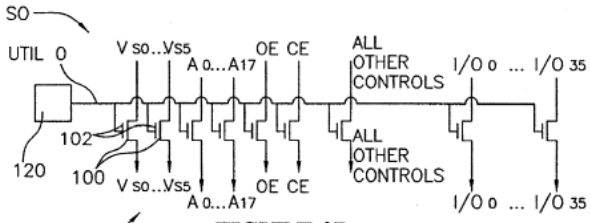


FIGURE 8B

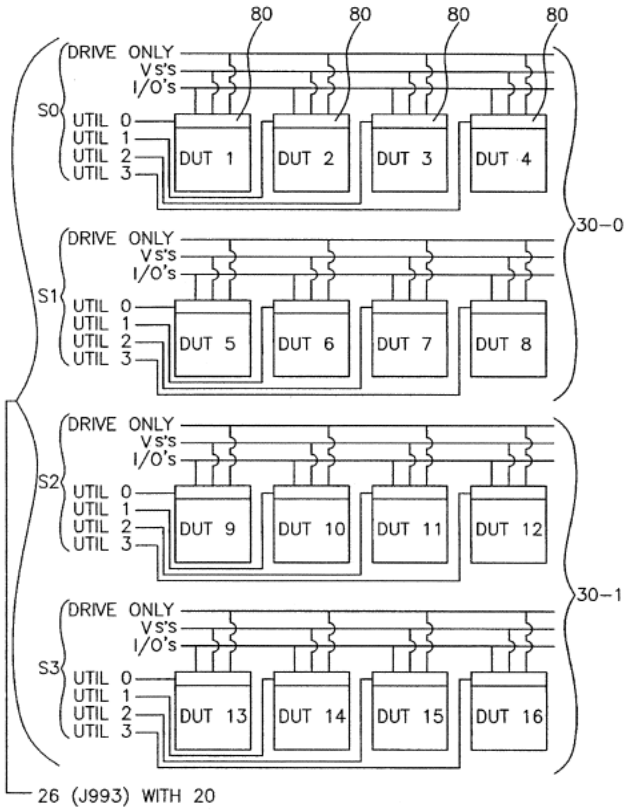


FIGURE 8D

Figure 8A, 8B and Figure 8D from the '112 patent.

96. [redacted]

[redacted]

97. Other related patents, such as US Patent 6,300,786 and US Patent 6,246,250, both filed by Micron, describe essentially the same technology [redacted].

98. ***Other Patents***. The solutions disclosed in other patents/patent applications referenced in the Blanchard and Schneck Declarations [redacted] These patents include:

- US patent 6,798,225, US patent 6,678,850, and US patent 6,784,674 by Form Factor.
- US patent 6,888,366 by Samsung.
- US patent application 2007/0165469.

99. ***Verigy's Kiowa ASIC***. The publicly disclosed Verigy Kiowa "resource sharing" ASIC described in the September 2005 Evaluation Engineering magazine article (Blanchard Decl., Ex. QQ), [redacted]

100. ***Discrete RF switches***. These types of switches, which are produced by [redacted]

101. Based on the public disclosure documents provided to me for my review, I conclude that while certain individual aspects of [redacted] may very well be public information, and the general resource sharing concept was well established, [redacted]

Appendix I. List of Declaration Exhibits

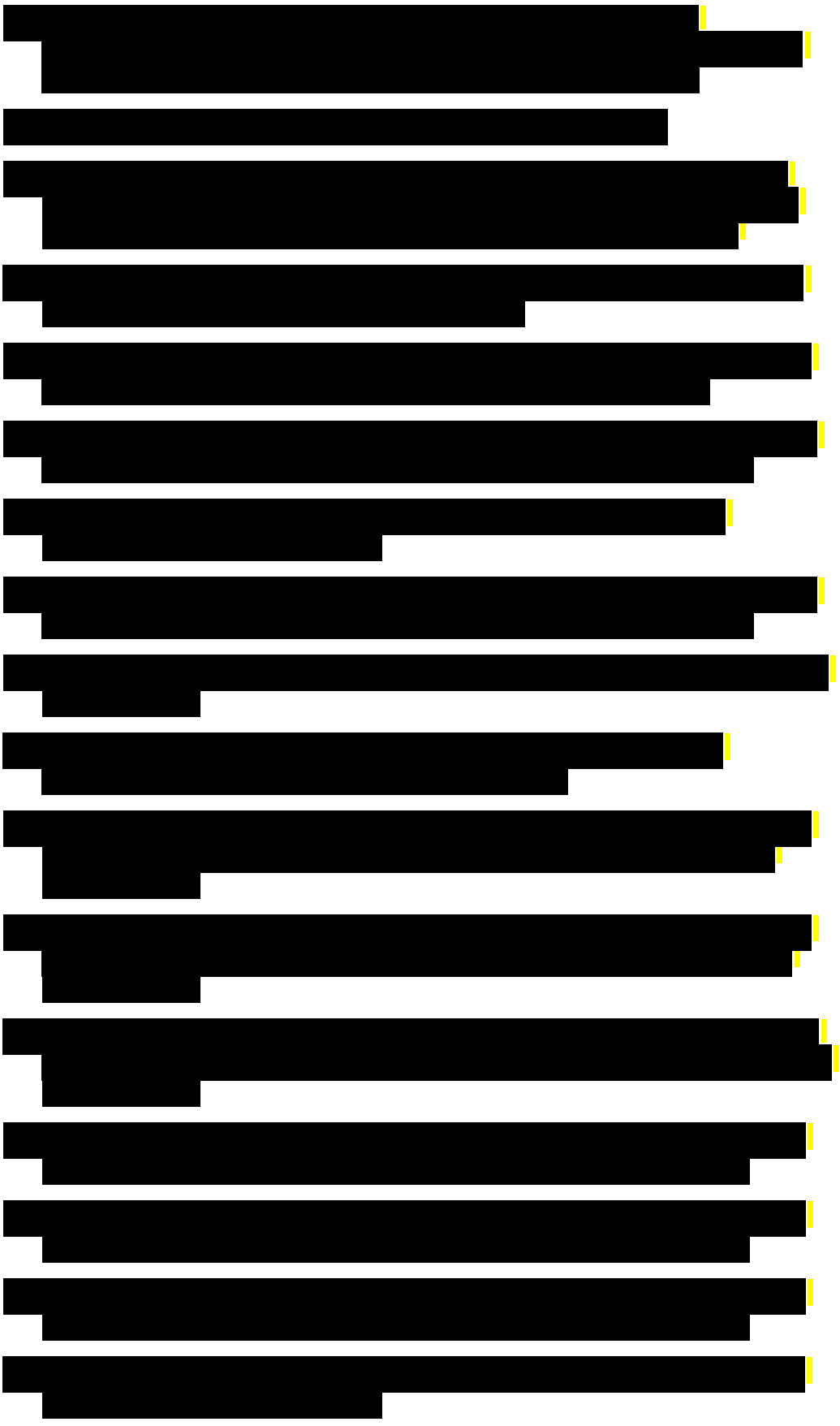
Exhibit A: Wei Wei's *curriculum vitae*

Exhibit B: SST49LF016C LPC 16 Mb Flash Memory Data Sheet

Exhibit C: Intel Serial Flash Memory Datasheet

Exhibit D:

Exhibit E:



[redacted]

Exhibit F:

[redacted]

Exhibit G:

[redacted]

Exhibit H:

[redacted]

[redacted]

Exhibit I: Declaration of Dr. Richard Blanchard – (selected exhibits)

[redacted]

ublication, Pub. No.: US2005/0237073/A1

[redacted]

Exhibit J: Declaration of Thomas Schneck, dated October 9, 2007 (including exhibits)

Exhibit K: Article entitled "Flash Memory Moves from Niche to Mainstream," published in the April/May 2006 issue of Chip Design Magazine

Appendix II. Verigy's Chameleon ASIC Development Timeline

Appendix III. STS Picasso ASIC Development Timeline

June 12, 2006

I declare under penalty of perjury under the laws of the United States that the foregoing is true and correct.

Executed this ____ day of November, 2007 at _____, California.

_____
Wei Wei